BIRCH, STEWART, KOLASCH & BIRCH, LLP

TERRELL C BIRCH
RAYMOND C STEWART
JOSEPH A KOLASCH
JAMES M SLATTERY
BERNARD L SWEENEY*
MICHAEL K MUTTER
CHARLES GORENSTEIN
GERALD M. MURPHY, JR
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MARC S. WEINER
JOE McKINNEY MUNCY
ROBERT J KENNEY
DONALD J DALEY
JOHN W. BAILEY
JOHN A CASTELLANO
GARY D YACURA

OF COUNSEL
HERBERT M BIRCH (1905-1996)
ELLIOT A GOLDBERG*
WILLIAM L GATES*
EDWARD H VALANCE
RUPERT J BRADY (RET)*
F. PRINCE BUTLER
FRED S WHISENHUNT

*ADMITTED TO A BAR OTHER THAN VA

INTELLECTUAL PROPERTY LAW
8110 GATEHOUSE ROAD
SUITE 500 EAST
FALLS CHURCH, VA 22042-1210
USA

(703) 205-8000

FAX (703) 205-8050
(703) 698-8590 (G IV)

e-mail: mailroom@bskb.com
web: http://www.bskb.com

CALIFORNIA OFFICE
COSTA MESA, CALIFORNIA

THOMAS S AUCHTERLONIE
JAMES T ELLER, JR
SCOTT L LOWE
MARK J NUELL, PH D
D RICHARD ANDERSON
PAUL C LEWIS
MARK W MILSTEAD*
RICHARD J GALLAGHER
JAYNE M SAYDAH*
MARYANNE ARMSTRONG, PH D
HYUNG N SOHN
ALAN PEDERSEN-GILES
KECIA J REYNOLDS

REG PATENT AGENTS
FREDERICK R. HANDREN
MAKI HATSUMI
MIKE S RYU
CRAIG A McROBBIE
GARTH M DAHLEN, PH D
ROBERT E GOOZNER, PH D
MATTHEW J LATTIG
TIMOTHY R WYCKOFF
KRISTI L RUPERT, PH D
LARRY J HUME
ALBERT K LEE
HRAYR A SAYADIAN, PH
EVE L FRANK, PH D.
MATTHEW T SHANLEY

Date: November 28, 2000

Docket No.: 0465-0758P

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): Jun Sik LEE

For: METHOD FOR FABRICATING CAPACITOR OF SEMICONDUCTOR DEVICE

Enclosed are:

- ☒ A specification consisting of thirteen (13) pages
- ☒ Six (6) sheet(s) formal drawings
- ☐ An assignment of the invention
- ☐ Applicant claims small entity status in accordance with 37 C.F.R. § 1.27
- ☒ Certified copy of Priority Document(s)
- ☒ Executed Declaration (☐ Original ☒ Photocopy)
- ☐ Application Data Sheet in accordance with 37 C.F.R. § 1.76
- ☒ Preliminary Amendment
- ☒ Information Disclosure Statement, PTO-1449 and reference(s)

☐ Other:

☐ Applicant requests early publication

The filing fee has been calculated as shown below:

			LARGE ENTITY	SMALL ENTITY
	BASIC FEE		**$710.00**	**$355.00**
	NUMBER FILED	NUMBER EXTRA	RATE FEE	RATE FEE
TOTAL CLAIMS	10- 20 =	0	X 18 = $0.00	x 9 = $0.00
INDEPENDENT CLAIMS	2- 3 =	0	x 80 = $0.00	x 40 = $0.00
☐ MULTIPLE DEPENDENT CLAIMS PRESENTED			+ $270.00	+ $135.00
		TOTAL	$710.00	$0.00

☒ A check in the amount of $710.00 to cover the filing fee and recording fee (if applicable) is enclosed.

☐ Please charge Deposit Account No. 02-2448 in the amount of $0.00. A triplicate copy of this transmittal form is enclosed.

☒ Please send correspondence to:

BIRCH, STEWART, KOLASCH & BIRCH, LLP **or** Customer No. 2292
P.O. Box 747
Falls Church, VA 22040-0747
Telephone: (703) 205-8000

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Gary D. Yacura, #35,416

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

GDY/MSR:ewd
0465-0758P
Attachments

(REV. 11/02/2000)

PATENT
0465-0758P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jun Sik LEE

Appl. No. NEW Group: Unknown

Filed: November 28, 2000 Examiner: Unknown

For: METHOD OF FABRICATING CAPACITOR OF SEMICONDUCTOR DEVICE

PRELIMINARY AMENDMENT

Assistant Commissioner
Washington, D.C. 20231

November 28, 2000

Dear Sir:

The following Preliminary Amendments and Remarks are respectfully submitted in conjunction with the above-identified application.

IN THE SPECIFICATION

Page 2

Line 3, change "1a to 1e" to --1A to 1E--.

Line 8, change "1a" to --1A--.

Line 15, change "1b" to --1B--.

Line 18, change "1c" to --1C--.

Page 3

Line 7, change "1d" to --1D--.

Line 15, change "1e" to --1E--.

Page 5

Line 13, change "1a to 1e" to --1A to 1E--.

Line 15, change "2a to 2E" to --2A to 2E--.

Line 20, change "2a to 2E" to --2A to 2E--.

Page 6

Line 20, change "2a" to --2A--.

Page 7

Line 12, change "2c" to --2C--.

Line 21, change "2c" to --2C--.

Page 8

Line 2, change "2d" to --2D--.

Line 10, change "2e" to --2E--.

Line 16, change "2e" to --2E--.

REMARKS

Claims 1-10 are pending in the present application. Claims 1 and 2 are in independent form.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly solicited.

In the event that any matters remain at issue in the application, the Examiner is invited to contact Mike S. Ryu, Reg. No. 38,604 at (703) 205-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____

Gary D. Yacura
Reg. No. 35,416

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

GDY/MSR:ewd

Atty Docket No. 465-758P

METHOD FOR FABRICATING CAPACITOR OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, and more particularly, to a method for fabricating a capacitor of a semiconductor device.

2. Background of Related Art

With high packing density of a DRAM, an area of a chip has been reduced and areas of a transistor and a capacitor have been also reduced. At this time, the capacitor includes a high dielectric film to increase capacitance in a small area. Ta_2O_5 or BST($Ba_xSr_{1-x}T_iO$) may be used as the high dielectric film To use the high dielectric film in the capacitor, a lower electrode resistant to oxidation and heat is required. Oxide-based materials, such as platinum(Pt), iridium(Ir), and ruthenium(Ru), may be used as the lower electrode. Among the materials, Ru or RuO_2, which can be deposited by chemical vapor deposition and can be easily etched to form a capacitor structure, is especially used as the material for the lower electrode. During an etching process to form the capacitor structure, the lower electrode is etched to form a concave structure to the effective area of the capacitor in a given area. To form such a concave structure, Pt may be used but has a drawback in that it is more expensive than Ru during chemical vapor deposition.

A related art method for fabricating a capacitor using Ru, RuO_2, or a metal material alloyed with Ru as a lower electrode will now be described with reference to the accompanying drawings.

Figs. 1a to 1e are sectional views showing a related art method for fabricating a capacitor of a semiconductor device.

A gate oxide film and a gate electrode are sequentially formed on some region of a semiconductor substrate, and source and drain regions are formed in the semiconductor substrate at both sides of the gate electrode (not shown).

As shown in Fig. 1a, an interleaving insulating film 11 is formed on the source region or the drain region to have a contact hole.

A polysilicon layer is then deposited on the interleaving insulating film 11 including the contact hole. A contact plug 12 is formed within the contact hole by polishing back the polysilicon layer.

Afterwards, a nitride film 13 is deposited on an entire surface including the contact plug 12, and an oxide film 14 is deposited on the nitride film 13.

As shown in Fig. 1b, the oxide film 14 and the nitride film 13 are sequentially etched by photolithography process to expose the contact plug 12 and the interleaving insulating film 11 adjacent to the contact plug 12.

As shown in Fig. 1c, a barrier film 15 is deposited on the contact plug 12 and the interleaving insulating film 11 including the oxide film 14 and the nitride film 13 to have a thickness of about 200A. A conductive layer 16 is then deposited on the barrier film 15 to have a thickness of about 200A.

The conductive layer 16 is formed of Ru, RuO_2, or a metal material alloyed with Ru. The barrier film 15 may be formed on only the contact plug 12 within the contact hole.

Afterwards, a photoresist 17 is deposited on the entire surface including the conductive layer 16 between the respective oxide films 14. The photoresist 17 is then etched back to expose sides of the conductive layer 16 between the respective oxide films 14 and an upper portion of the conductive layer 16 on the oxide film 14.

The conductive layer 16 on the oxide film 14 and the barrier film 15 are sequentially removed using the photoresist 17 as a mask, so that a pair of U-shaped barrier film 15 and lower electrode 16a are formed, as shown in Fig. 1d, to be isolated from another pair of U-shaped barrier film 15 and lower electrode 16a.

As described above, cells are separated from one another by isolating the lower electrodes 16a from one another.

The lower electrodes 16a are etched by $Ar+Cl_2$ plasma gas.

The photoresist 17 is then removed using O_2 plasma gas.

At this time, Ru or RuO_2 of the lower electrodes 16a reacts with O_2 gas so that a volatile gas of RuO_4 is generated. For this reason, the lower electrodes 16a may be damaged.

Next, as shown in Fig. 1e, the oxide film 14 and the nitride film 13 between the respective lower electrodes 16a are sequentially removed, and a high dielectric film 18 and a conductive layer are sequentially formed on the entire surface including the lower electrodes 16a. The conductive layer and the high dielectric film 18 are partially removed to isolate a pair of the conductive layer and high dielectric film from a neighboring pair of the conductive layer and high dielectric film. Thus, a U-shaped capacitor which includes an upper electrode 19, the high dielectric film 18 and the lower electrode 16a is completed.

The aforementioned related art method for fabricating a capacitor of a semiconductor device has several problems.

When the photoresist used as a mask to form the lower electrode of Ru or RuO_2 in a U-shape is removed by O_2 plasma gas, O_2 gas chemically reacts with the lower electrode. As a result, the lower electrode is damaged, thereby reducing process yield.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a method for fabricating a capacitor of a semiconductor device that substantially obviates one or more of the problems occurring in the related art.

An object of the present invention is to provide a method for fabricating a capacitor of a semiconductor device in which loss of a lower electrode is minimized so as to improve process yield.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a method for fabricating a capacitor of a semiconductor device includes: forming a conductive region on a region of a semiconductor substrate; forming an interleaving insulating film having a contact hole in the conductive region; forming a contact plug within the contact hole; forming insulating film patterns on a region of the interleaving insulating film to expose the contact plug and the interleaving insulating film adjacent to the contact plug; depositing a barrier film and a first conductive layer on an entire surface

including the contact plug and the insulating film patterns; forming a photoresist on an upper portion of the contact plug between the insulating film patterns; sequentially removing the first conductive layer and the barrier film on the insulating film patterns using the photoresist as a mask to form a lower electrode and a barrier film in a U-shape; removing the photoresist using a non-reactive etching method; removing the insulating film patterns; and sequentially forming a dielectric film and an upper electrode on surfaces of the lower electrode and the barrier film.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

Figs. 1a to 1e are sectional views of process steps showing a related art method for fabricating a capacitor of a semiconductor device; and

Figs. 2a to 2e are sectional views of process steps showing a method for fabricating a capacitor of a semiconductor device according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Figs. 2a to 2e are sectional views of process steps showing a method for fabricating a capacitor of a semiconductor device according to the present invention.

The method for fabricating a capacitor of a semiconductor device according to the present invention is performed in such a manner that a conductive layer is deposited on a semiconductor substrate (not shown). A photoresist pattern is then formed on the conductive layer, and the conductive layer is etched using the photoresist as a mask to form a lower electrode. The photoresist is then removed using an etching gas having no volatility with respect to the lower electrode, and a dielectric film and an upper electrode are thereafter sequentially formed on a surface of the lower electrode.

In other words, the lower electrode of Ru, RuO_2, or a metal material alloyed with Ru is removed using the photoresist as a mask, and then the photoresist is removed using the etching gas having no volatility when reacting with the lower electrode.

One of H_2O, NH_3, and N_2 may be used as the etching gas. Alternatively, a gas mixture of H_2 and O_2 in which an amount of H_2 is smaller than an amount of O_2, may be used as the etching gas. Further, a mixing gas of H_2O, NH_3, and N_2, a gas mixture of N_2 and NH_3, a gas mixture of NH_3 and H_2O, or a gas mixture of N_2 and H_2O may be used as the etching gas.

The aforementioned method for fabricating a capacitor of a semiconductor device according to the present invention will be described below in more detail.

A gate oxide film and a gate electrode are sequentially formed on a region of a semiconductor substrate, and source and drain regions are formed in the semiconductor substrate at both sides of the gate electrode (not shown).

Next, as shown in Fig. 2a, an interleaving insulating film 101 is formed over the source region or the drain region with a contact hole formed therein.

A conductive material such as polysilicon or tungsten, or another conductive material having low resistance is then deposited on the interleaving insulating film 101 includingin the contact hole.

A contact plug 102 is formed within the contact hole by an etch-back process or a chemical mechanical polishing process so that the conductive material is only formed within the contact hole.

Afterwards, a nitride film 103 is deposited on interleaving insulating film 101 including the contact plug 102, and an oxide film 104 is deposited on the nitride film 103 by, for example, chemical vapor deposition. The nitride film 103 has a thickness of about 500A.

A photoresist (not shown) is deposited on the oxide film 104 and then selectively patterned by exposure and developing processes, so that the photoresist over the contact plug 102 and the interleaving insulating film 101 adjacent to the contact plug 102 is removed.

The oxide film 104 and the nitride film 103 are sequentially etched as seen in Fig. 2B using the patterned photoresist as a mask so as to expose the contact plug 102 and the interleaving insulating film 101 adjacent to the contact plug 102.

As shown in Fig. 2c, a barrier film 105 and a conductive layer 106 are sequentially deposited over the contact plug 102 and the interleaving insulating film 101 including the oxide film 104 and the nitride film 103 to have a thickness of about 200A.

At this time, the barrier film 105 acts to closely adhere the conductive layer 106 and the oxide film 104 to each other, and alternatively may be formed on only the contact plug 102 within the contact hole. The conductive layer is formed of Ru, RuO_2, or a metal material alloyed with Ru.

Afterwards, a photoresist 107 is deposited on the resultant surface including the conductive layer 106 between the respective oxide films 104. The photoresist 107 is then etched back to expose sides of the conductive layer 106 between the respective oxide films 104 and an upper portion of the conductive layer 106 on the oxide film 104. See Fig. 2c.

Portions of the conductive layer 106 and the barrier film 105 are sequentially removed using the etched back photoresist 107 as a mask to expose the upper portion of the oxide film 104, so that

U-shaped (as seen in cross-section) barrier films 105 and lower electrodes 106a isolated from another U-shaped barrier films 105 and lower electrodes 106a are formed as shown in Fig. 2d.

As described above, cells are separated from one another by isolating the lower electrodes 106a from one another. The lower electrodes 106a are etched by, for example, $Ar+Cl_2$ plasma gas.

The photoresist 107 is then removed using an etching gas that does not react with the metal material of the lower electrode 106a. One of H_2O, NH_3, and N_2 may be used as the etching gas. Alternatively, a gas mixture of H_2 and O_2 in which an amount of H_2 is smaller than an amount of O_2, may be used as the etching gas. Also, a mixture of H_2O, NH_3, and N_2, a mixture of N_2 and NH_3, a mixure of NH_3 and H_2O, or a mixture of N_2 and H_2O may be used as the etching gas.

Next, as shown in Fig. 2e, the oxide film 104 and the nitride film 103 between the respective lower electrodes 106a are removed, and a high dielectric film 108 and a conductive layer are sequentially formed on the resultant surface including the lower electrodes 106a. Portions of the conductive layer and the high dielectric film 108 are removed to electrically isolate a respective conductive layer/ high dielectric film unit from a neighboring conductive layer/high dielectric film unit. Thus, the high dielectric film 108 and an upper electrode 109 are sequentially formed.

Specifically, as seen in Fig. 2e, after the conductive layer is formed of Ru, RuO_2, or a metal material alloyed with Ru, the photoresist is deposited to form the upper electrodes 109 isolated from one another and then selectively patterned. The conductive layer is removed using the patterned photoresist as a mask to form the upper electrodes 109 isolated from one another. The patterned photoresist is removed using the same etching gas of the lower electrode 106a. Thus, a capacitor which includes the upper electrode 109, the high dielectric film 108 and the lower electrode 106a is completed.

As aforementioned, the method for fabricating a capacitor of a semiconductor substrate according to the present invention has the following advantages.

Since the photoresist used as a mask to etch the lower electrode of Ru, RuO_2 or a metal material alloyed with Ru is removed using an etching gas that does not react with the lower electrode, the lower electrode is prevented from being damaged, thereby improving process yield.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.

WHAT IS CLAIMED IS:

1. A method for fabricating a capacitor of a semiconductor device comprising:

depositing a conductive layer on a substrate;

forming a photoresist pattern on the conductive layer;

etching the conductive layer using the photoresist pattern as a mask to form a lower electrode;

removing the photoresist using an etching gas that is non-reactive with respect to the lower electrode; and

forming a dielectric film and an upper electrode on a surface of the lower electrode.

2. The method of claim 1, wherein the upper and lower electrodes are one of Ru, RuO_2, and a metal material alloyed with Ru.

3. The method of claim 1, wherein the etching gas is one of H_2O, NH_3, and N_2, a mixture of H_2 and O_2 in which an amount of H_2 is smaller than an amount of O_2, a mixture of H_2O, NH_3, and N_2, a mixture of N_2 and NH_3, a mixture of NH_3 and H_2O, and a mixture of N_2 and H_2O.

4. A method for fabricating a capacitor of a semiconductor device comprising:

forming a conductive region on a semiconductor substrate;

forming an interleaving insulating film having a contact hole therein over the conductive region;

forming a contact plug within the contact hole;

forming insulating film patterns on of the interleaving insulating film to expose the contact plug and the interleaving insulating film adjacent to the contact plug,

depositing a barrier film and a first conductive layer on the contact plug and the insulating film patterns;

forming a photoresist over the contact plug between the insulating film patterns;

sequentially removing the first conductive layer and the barrier film on the insulating film patterns using the photoresist as a mask, thereby forming a lower electrode and a barrier film in a U-shape in cross-section;

removing the photoresist using an etching gas that is non-reactive with respect to the lower electrode;

removing the insulating film patterns; and

sequentially forming a dielectric film and an upper electrode on the lower electrode and the barrier film.

5. The method of claim 4, wherein the lower electrode is oneof Ru, RuO_2 and a metal material alloyed with Ru.

6. The method of claim 4, wherein the etching gas is one of H_2O, NH_3, and N_2; a mixture of H_2 and O_2 in which an amount of H_2 is smaller than an amount of O_2, a mixture of H_2O, NH_3, and N_2, a mixture of N_2 and NH_3, a mixture of NH_3 and H_2O, or a mixture of N_2 and H_2O is used as the etching gas.

7. The method of claim 4, wherein the insulating film pattern comprises an oxide film.

8. The method of claim 4, wherein the insulating film pattern is formed by stacking two insulating films.

9. The method of claim 8, wherein the two insulating films are a nitride film and an oxide film.

10. The method of claim 4, wherein the barrier film is only formed on the contact plug within the contact hole.

ABSTRACT OF THE DISCLOSURE

A method for fabricating a capacitor of a semiconductor device is disclosed, in which loss of and damage to a lower electrode is minimized to improve process yield. The method for fabricating a capacitor of a semiconductor device includes, for example, forming a conductive region on a semiconductor substrate; forming an interleaving insulating film having a contact hole on the conductive region; forming a contact plug within the contact hole; forming insulating film patterns on some region of the interleaving insulating film to expose the contact plug and the interleaving insulating film adjacent to the contact plug; depositing a barrier film and a first conductive layer on an entire surface including the contact plug and the insulating film patterns; forming a photoresist on an upper portion of the contact plug between the insulating film patterns; sequentially removing portions of the first conductive layer and the barrier film on the insulating film patterns using the photoresist as a mask to form a lower electrode and a barrier film in a U-shape in cross-section; removing the photoresist using an etching gas that is non-reactive with respect to the lower electrode; removing the insulating film patterns; and sequentially forming a dielectric film and an upper electrode on surfaces of the lower electrode and the barrier film.

FIG . 1A
Related Art

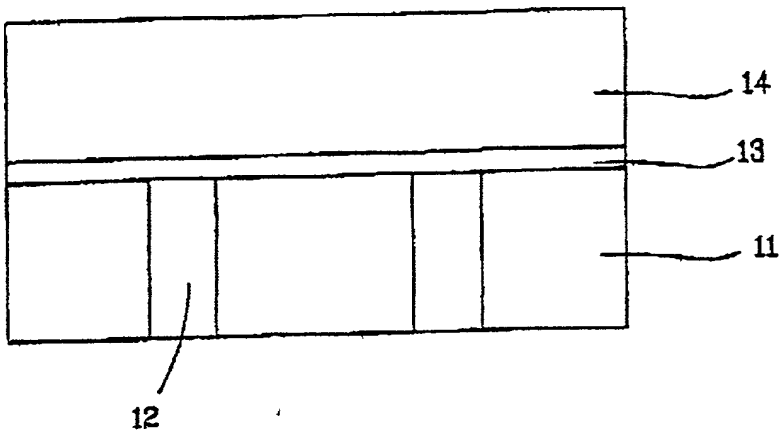


FIG . 1B
Related Art

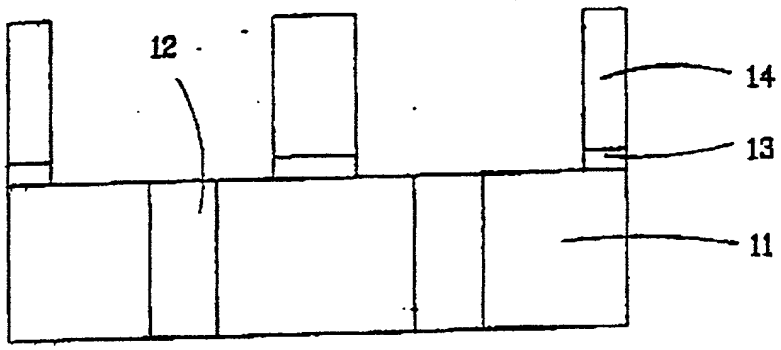


FIG . 1C
Related Art

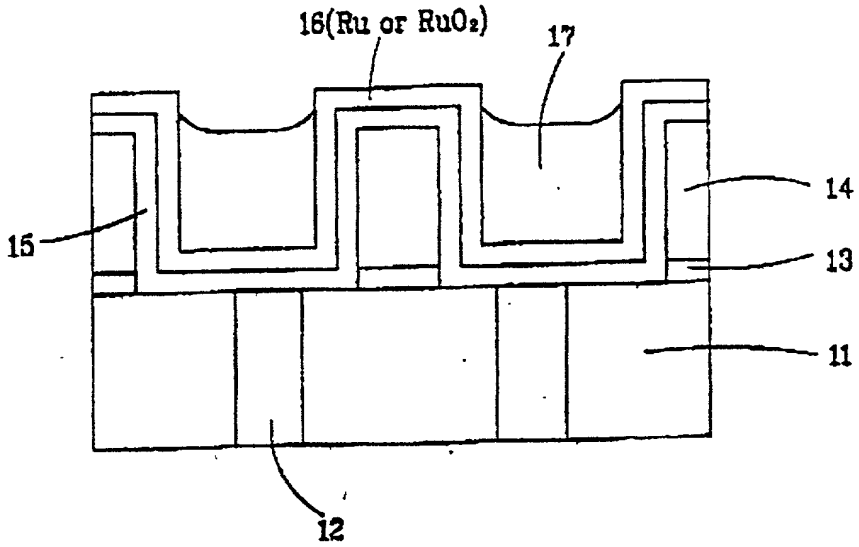


FIG . 1D
Related Art

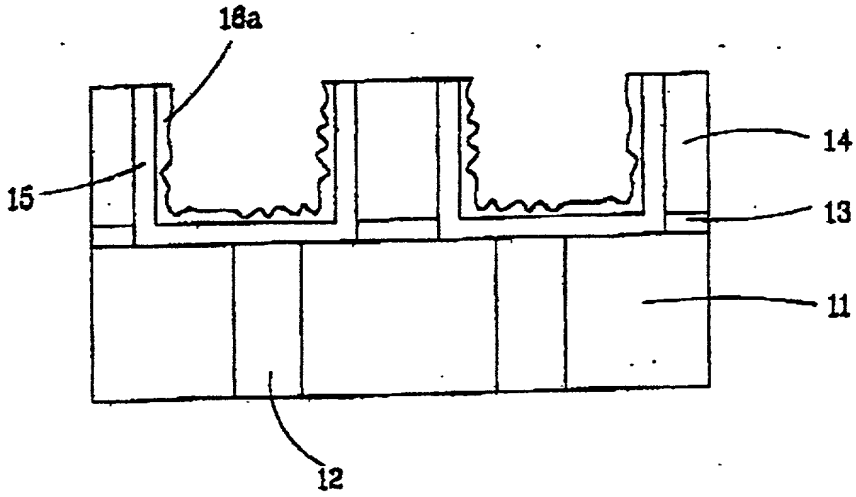


FIG . 1E
Related Art

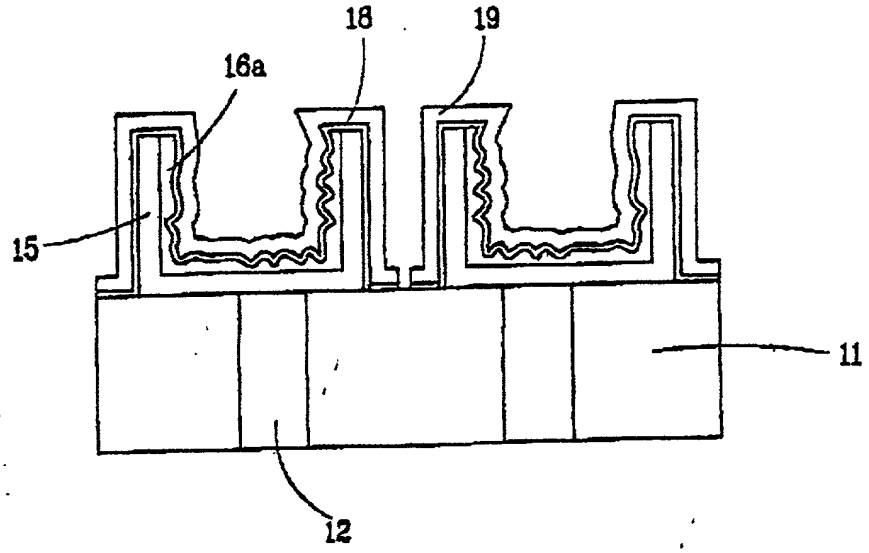


FIG . 2A

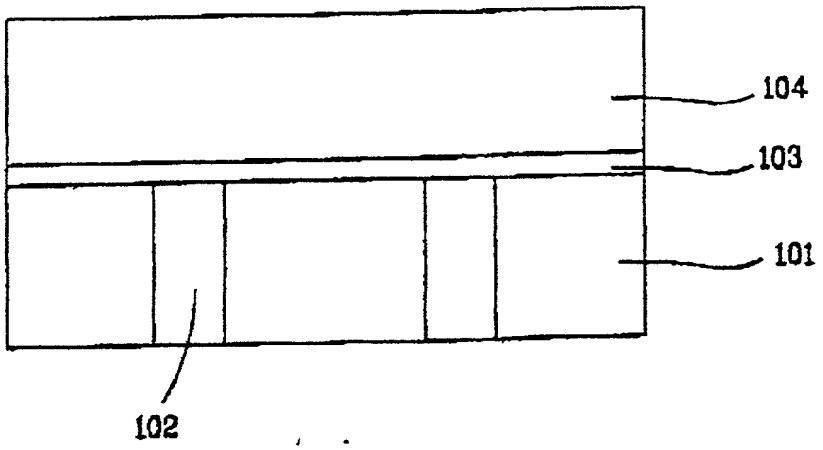


FIG . 2B

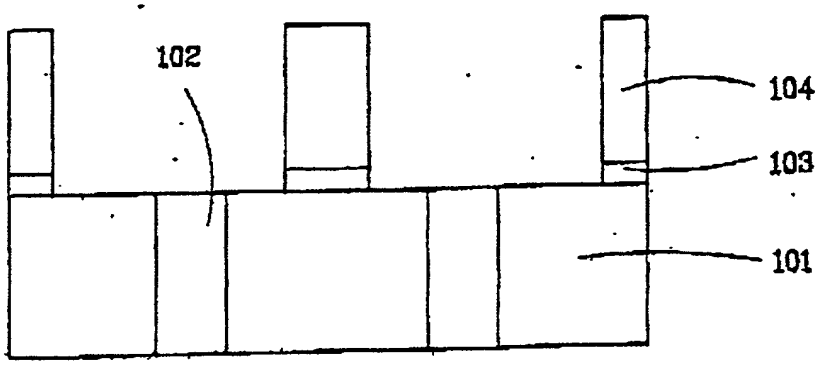


FIG . 2C

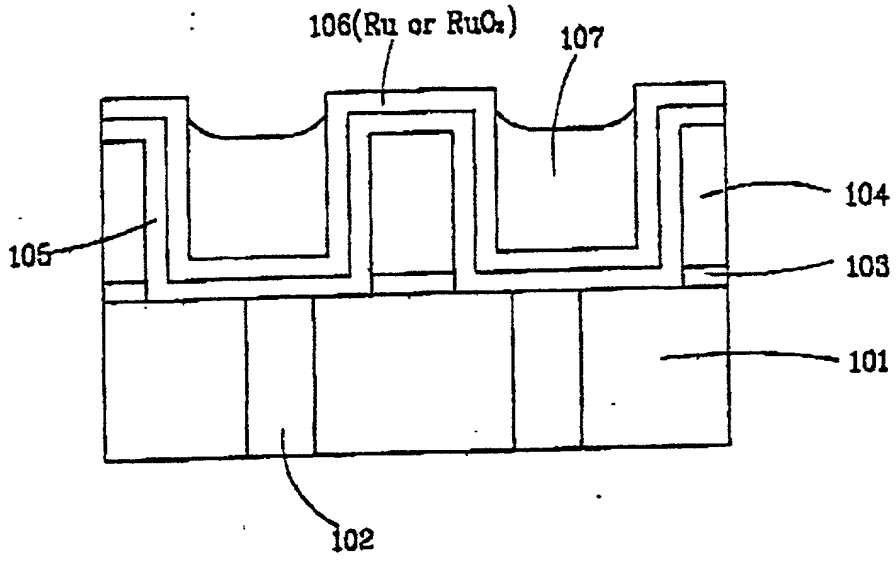

106(Ru or RuO2)
107
104
105
103
101
102

FIG . 2D

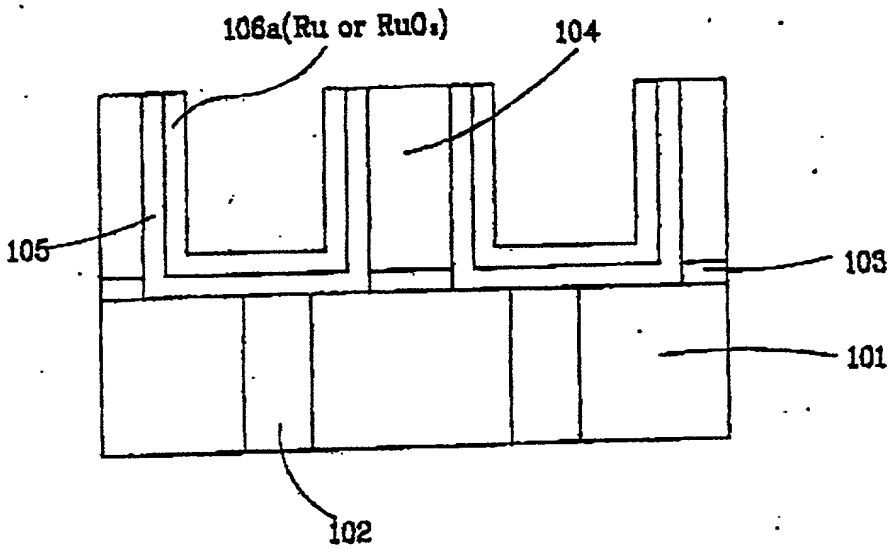
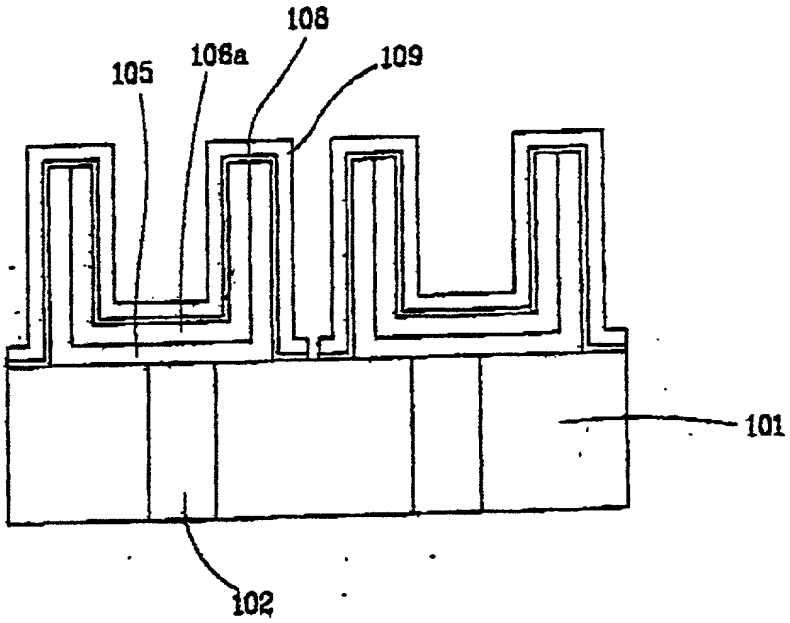

106a(Ru or RuO2)
104
105
103
101
102

FIG . 2E



Attorney Docket No.

BIRCH, STEWART, KOLASCH & BIRCH, LLP

P.O. Box 747 Falls Church, Virginia 22040-0747

Telephone: (703) 205-8000 Facsimile: (703) 205-8050

EASE NOTE:
)U MUST
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COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

sert Title — METHOD FOR FABRICATING CAPACITOR OF SEMICONDUCTOR DEVICE

l in Appropriate formation - e Use Without ecification tached.

the specification of which is attached hereto. If not attached hereto,

the specification was filed on _____ as
United States Application Number _____;
and amended on _____ (if applicable) and/or
the specification was filed on _____ as PCT
International Application Number _____; and was
amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, .56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, 19(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

sert Priority formation: appropriate) Prior Foreign Application(s) (Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed Yes	No
2000-47542	Korea	August / 17 / 2000	☒	☐
			☐	☐
			☐	☐
			☐	☐

I hereby claim the benefit under Title 35, United States Code, 19(e) of any United States provisional applications(s) listed below.

sert Provisional pplication(s) any) (Application Number)	(Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

sert Requested formation: appropriate) Country	Application Number	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, 20 of any United States and/or PCT application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, 12, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, .56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

sert Prior U.S. pplication(s): any) (Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

Attorney Docket No.

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

Raymond C. Stewart	(Reg. No. 21,066)	Terrell C. Birch	(Reg. No. 19,382)
Joseph A. Kolasch	(Reg. No. 22,463)	James M. Slattery	(Reg. No. 28,380)
Bernard L. Sweeney	(Reg. No. 24,448)	Michael K. Mutter	(Reg. No. 29,680)
Charles Gorenstein	(Reg. No. 29,271)	Gerald M. Murphy, Jr.	(Reg. No. 28,977)
Leonard R. Svensson	(Reg. No. 30,330)	Terry L. Clark	(Reg. No. 32,644)
Andrew D. Meikle	(Reg. No. 32,868)	Marc S. Weiner	(Reg. No. 32,181)
Joe McKinney Muncy	(Reg. No. 32,334)	Donald J. Daley	(Reg. No. 34,313)
John W. Bailey	(Reg. No. 32,881)	John A. Castellano	(Reg. No. 35,094)
Gary D. Yacura	(Reg. No. 35,416)		

Send Correspondence to:

BIRCH, STEWART, KOLASCH & BIRCH, LLP or **Customer No. 2292**
P.O. Box 747 Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 Facsimile: (703) 205-8050

LEASE NOTE: OU MUST OMPLETE HE OLLOWING: ↓

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

ll Name of First or Sole Inventor; Insert Name of Inventor; Insert Date This Document is Signed →
Insert Residence; Insert Citizenship →
Insert Post Office Address →

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Jun Sik LEE	Jun Sik Lee	11/27/2000
Residence (City, State & Country): Chungcheongbuk-do, Korea	CITIZENSHIP: Republic of Korea	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country): Sungwoon APT., 102-805, 660-44, Yulryang-dong, Sangdang-ku, Cheongju-si, Chungcheongbuk-do, Korea		

ll Name of Second Inventor, if any; see above

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)	CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		

ll Name of Third Inventor, if any; see above

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)	CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		

ll Name of Fourth Inventor, if any; see above

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)	CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		

ll Name of Fifth Inventor, if any; see above

GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)	CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		

*DATE OF SIGNATURE